Interview Summary	Application No.	Applicant(s)	
	10/828,542	MCKINZIE, WILLIAM E.	
	Examiner	Art Unit	
	Seungsook Ham	2817	

All participants (applicant, applicant's representative, PTO personnel):

(1) *Seungsook Ham*. (3)_____.

(2) *Alan C. Gordon*. (4)_____.

Date of Interview: *04 May 2006*.

Type: a)☒ Telephonic b)☐ Video Conference
c)☐ Personal [copy given to: 1)☐ applicant 2)☐ applicant's representative]

Exhibit shown or demonstration conducted: d)☐ Yes e)☒ No.
If Yes, brief description: _____.

Claim(s) discussed: *1-78 (proposed amendment)*.

Identification of prior art discussed: *N/A*.

Agreement with respect to the claims f)☐ was reached. g)☒ was not reached. h)☐ N/A.

Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: *The examiner indicated that the proposed amendment will not be entered since the newly added limitation raises new issues. The applicant suggested amending the claims that the examiner indicated as allowable subject matter in the final office action*.

(A fuller description, if necessary, and a copy of the amendments which the examiner agreed would render the claims allowable, if available, must be attached. Also, where no copy of the amendments that would render the claims allowable is available, a summary thereof must be attached.)

THE FORMAL WRITTEN REPLY TO THE LAST OFFICE ACTION MUST INCLUDE THE SUBSTANCE OF THE INTERVIEW. (See MPEP Section 713.04). If a reply to the last Office action has already been filed, APPLICANT IS GIVEN A NON-EXTENDABLE PERIOD OF THE LONGER OF ONE MONTH OR THIRTY DAYS FROM THIS INTERVIEW DATE, OR THE MAILING DATE OF THIS INTERVIEW SUMMARY FORM, WHICHEVER IS LATER, TO FILE A STATEMENT OF THE SUBSTANCE OF THE INTERVIEW. See Summary of Record of Interview requirements on reverse side or on attached sheet.

Examiner Note: You must sign this form unless it is an Attachment to a signed Office action.

_____
Examiner's signature, if required

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)
In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

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Facsimile Transmittal

CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 CFR 1.6(d)

I hereby certify that this paper and the attached papers are being transmitted by facsimile to the Patent and Trademark Office, 571-273-2405, on this date:

05/03/2006
Date

Michelle Mebarak

To: Examiner Seungsook Ham
USPTO

Telephone: 571-272-2405 **Fax:** 571-273-2405

From: Alan C. Gordon
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No. of Pages: 15 (including cover)
Date: May 3, 2006

42372.0004 (4786)

Message:

Transmitted herewith, for your review, are the Applicant's proposed claim amendments. I look forward to speaking with you regarding this application tomorrow at 1:00 EST.

Document6
5/3/06 3:00 PM ()

DO NOT ENTER

5/4/06

U.S.S.N. 10/828,542
W. McKinzie

Proposed Amendment
Do NOT enter
5/4/06
EJ

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in this application. Added text is indicated by underlining, and deleted text is indicated by ~~strikethrough~~. Changes are identified by a vertical bar in the margin.

1. (Currently amended) A cluster resonator, comprising:

a first conducting plane;

a second substantially parallel conducting plane;

a cluster of vias of essentially uniform length oriented substantially normal to the conducting planes, each via in the cluster comprising a first end and a second end;

a first conducting pad disposed in a third plane substantially parallel and capacitively coupled to the first conducting plane and physically coupled with the vias of the cluster of vias proximate their first ends; and

a second conducting pad disposed in a fourth plane substantially parallel and capacitively coupled to the second conducting plane and physically coupled with the vias of the cluster of vias proximate their second ends, wherein the vias are physically connected to only the first and second conducting pads;

wherein a preselected reactance of the cluster resonator forms, over a desired frequency range, an electromagnetic shunt circuit between the first and second conducting planes.

2. (Canceled)

3. (Currently amended) The cluster resonator of claim ~~2~~1, wherein the vias of the cluster of vias are disposed along a perimeter that defines a substantially field free ~~an~~ interior region.

4. (Currently amended) The cluster resonator of claim 3, wherein one or more electrically isolated interior vias comprising portions of transmission lines are routed within the interior region of the cluster of vias.

5. (Canceled)

6. (Original) The cluster resonator of claim 1, wherein the first conducting pad is external relative to the first and second conducting planes.

7. (Original) The cluster resonator of claim 1, wherein the first conducting pad is internal relative to the first and second conducting planes.

8. (Original) The cluster resonator of claim 1, wherein the second conducting pad is external relative to the first and second conducting planes.

9. (Original) The cluster resonator of claim 1, wherein the second conducting pad is internal relative to the first and second conducting planes.

10. (Original) The cluster resonator of claim 1, wherein the first and second conducting pads are internal relative to the first and second conducting planes.

11. (Original) The cluster resonator of claim 1, wherein the first and second conducting pads are external relative to the first and second conducting planes.

12. (Previously presented) The cluster resonator of claim 1, wherein its topology comprises a mechanically balanced structure.

13. (Previously presented) The cluster resonator of claim 1, wherein the first and second conducting planes are metallic layers incorporated with a multi-layered panel circuit.

14. (Previously presented) The cluster resonator of claim 13, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

15. (Previously presented) The cluster resonator of claim 13, wherein the multi-layered panel circuit is a multi-chip module.

16. (Previously presented) The cluster resonator of claim 13, wherein the multi-layered panel circuit is a semiconductor chip.

17. (Original) The cluster resonator of claim 3, wherein the cluster of vias is disposed along a circular path.

18. (Original) The cluster resonator of claim 3, wherein the cluster of vias is disposed along an elliptical path.

19. (Original) The cluster resonator of claim 3, wherein the cluster of vias is disposed along a polygonal path.

20. (Previously presented) The cluster resonator of claim 4, wherein spacing of vias within the cluster of vias effects a Faraday cage that substantially shields the interior region from RF fields propagating within the first and second conducting planes.

21. (Previously presented) The cluster resonator of claim 20, wherein spacing of the vias within the cluster of vias in relation to the interior vias effects a predetermined line impedance in the interior vias.

22. (Currently amended) A cluster resonator, comprising:

a first conducting plane;

a second substantially parallel conducting plane;

a cluster of vias of essentially uniform length oriented substantially normal to the conducting planes, each via in the cluster comprising a first end and a second end;

first ends of each via in the cluster of vias coupled with the first conducting plane; and

a first conducting pad disposed in a third plane parallel and external to a region between the first and second conducting planes and capacitively coupled to the second conducting plane and physically coupled to each via in the cluster of vias proximate their second ends, wherein the vias in the

cluster of vias are physically connected to only the first conducting plane and the first conducting pad;

wherein a preselected reactance of the cluster resonator forms, over a desired frequency range, an electromagnetic shunt circuit between the first and second conducting planes.

23. (Canceled)

24. (Previously presented) The cluster resonator of claim 22, wherein the vias of the cluster of vias are disposed along a perimeter that defines a substantially field free interior region.

25. (Currently amended) The cluster resonator of claim 24, wherein one or more electrically isolated interior vias comprising portions of transmission lines are routed within the internal region of the cluster of vias.

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Previously presented) The cluster resonator of claim 22 comprising a second cluster of vias, each via in the second cluster of vias comprising a first end and a second end, wherein the vias in the second cluster of vias are coupled proximate their first ends to the second conducting plane and proximate their second ends to a second conducting

pad disposed in a fourth plane parallel and external to a region between the first and second conducting planes and capacitively coupled to the first conducting plane, wherein the vias in the cluster of vias are physically connected to only the second conducting plane and the second conducting pad.

30. (Canceled)

31. (Currently amended) The cluster resonator of claims 29 ~~and~~ or 30, wherein its topology comprises a mechanically balanced structure.

32. (Previously presented) The cluster resonator of claim 22, wherein the first and second conducting planes are metallic layers incorporated with a multi-layered panel circuit.

33. (Previously presented) The cluster resonator of claim 32, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

34. (Previously presented) The cluster resonator of claim 22, wherein the multi-layered panel circuit is a multi-chip module.

35. (Previously presented) The cluster resonator of claim 22, wherein the multi-layered panel circuit is a semiconductor chip.

36. (Original) The cluster resonator of claim 24, wherein the cluster of vias is disposed along a circular path.

37. (Original) The cluster resonator of claim 24, wherein the cluster of vias is disposed along an elliptical path.

38. (Original) The cluster resonator of claim 24 wherein the cluster of vias is disposed along a polygonal path.

39. (Previously presented) The cluster resonator of claim 25, wherein spacing of the vias of the cluster of vias effects a Faraday cage that substantially shields the interior region from RF fields propagating within the first and second conducting planes.

40. (Previously presented) The cluster resonator of claim 39, wherein spacing of the vias of the cluster of vias in relation to the interior vias effects a predetermined line impedance in the interior vias.

41. (Canceled)

42. (Previously presented) The cluster resonator of claim 1, further comprising a plurality of resonant vias and associated first and second conducting pads disposed in a periodic array associated with the first and second conducting planes.

43. (Previously presented) The cluster resonator of claim 22, further comprising a plurality of resonant vias and associated first conducting pads disposed in a periodic array associated with the first and second conducting planes.

44. (Currently amended) ~~An apparatus for suppressing electromagnetic interference~~ A cluster resonator comprising:

a first conducting pad;

a second substantially parallel conducting pad; and

a cluster of vias of essentially uniform length disposed between and oriented substantially normal to the conducting pads, each via of the cluster of vias having a first end and a second end, wherein the first and second ends are physically connected respectively to the first and second conducting pads;

wherein the vias of the cluster of vias are disposed along a perimeter thereby forming a substantially field free interior region therewithin; and

wherein one or more electrically isolated interior vias traverse the interior region of the cluster of vias, the interior vias comprising portions of transmission lines for passing electrical signals therethrough.

45. (Currently amended) The cluster resonator~~apparatus~~ of claim 44 wherein a spacing of the vias of the cluster of vias in relation to the interior vias is selected to effect a predetermined line impedance in the interior vias.

46. (Currently amended) The cluster resonator~~apparatus~~ of claim 44, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

47. (Previously presented) The cluster resonator of claim 1, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

48. (Previously presented) The cluster resonator of claim 22, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

49. (Currently amended) The cluster resonator ~~apparatus~~ of claim 44, wherein the cluster of vias is disposed along a circular path.

50. (Currently amended) The cluster resonator~~apparatus~~ of claim 44, wherein the cluster of vias is disposed along an elliptical path.

51. (Currently amended) The cluster resonator ~~apparatus~~ of claim 44, wherein the cluster of vias is disposed along a polygonal path.

52. (Currently amended) The cluster resonatorapparatus of claim 44, wherein the first and second conducting pads are metallic layers incorporated within a multi-layered panel circuit.

53. (Currently amended) The cluster resonator~~apparatus~~ of claim 52, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

54. (Currently amended) The cluster resonator~~apparatus~~ of claim 52, wherein the multi-layered panel circuit is a multi-chip module.

55. (Currently amended) The cluster resonatorapparatus of claim 52, wherein the multi-layered panel circuit is a semiconductor chip.

56. (Currently amended) A cluster resonator ~~An apparatus for suppressing electromagnetic radiation~~ comprising:

a first conducting plane;

a first substantially parallel conducting pad;

a cluster of vias oriented substantially normal to the first conducting plane and first conducting pad and disposed therebetween, each via of the cluster having a first end and a second end, wherein the first and second ends are physically connected respectively to the first conducting plane and first conducting pad;

wherein the vias of the cluster of vias are disposed along a perimeter thereby forming a substantially field free interior region therewithin; and

wherein one or more electrically isolated interior vias traverse the interior region of the cluster of vias, the interior vias comprising portions of transmission lines for passing electrical signals therethrough.

57. (Currently amended) The cluster resonatorapparatus of claim 56 wherein a spacing of the vias of the cluster of vias in relation to the interior vias is selected to effect a predetermined line impedance in the interior vias.

58. (Currently amended) The cluster resonatorapparatus of claim 56, wherein a diameter of the vias of the cluster of vias is selected to effect a predetermined inductance.

59. (Currently amended) The cluster resonatorapparatus of claim 56, wherein the cluster of vias is disposed along a circular path.

60. (Currently amended) The cluster resonatorapparatus of claim 56, wherein the cluster of vias is disposed along an elliptical path.

61. (Currently amended) The cluster resonatorapparatus of claim 56 wherein the cluster of vias is disposed along a polygonal path.

62. (Currently amended) The cluster resonatorapparatus of claim 56, wherein the first conducting plane and first conducting pad are metallic layers incorporated within a multi-layered panel circuit.

63. (Currently amended) The cluster resonatorapparatus of claim 62, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

64. (Currently amended) The cluster resonatorapparatus of claim 62, wherein the multi-layered panel circuit is a multi-chip module.

65. (Currently amended) The cluster resonatorapparatus of claim 62, wherein the multi-layered panel circuit is a semiconductor chip.

66. (Currently amended) The cluster resonatorapparatus of claim 56 further comprising a second conducting plane substantially parallel to the first conducting plane wherein the first conducting pad is external to the

region between the first and second conducting planes and capacitively coupled to the second conducting plane.

67. (Currently amended) The cluster resonatorapparatus of claim 56 further comprising a second conducting plane substantially parallel to the first conducting plane wherein the first conducting pad is internal to the region between the first and second conducting planes and capacitively coupled to the second conducting plane.

68. (Currently amended) A cluster resonator comprising:

a first conducting plane;

a second substantially parallel conducting plane;

a first conducting pad disposed in a third substantially parallel plane internal to the region between the first and second conducting planes;

a first cluster of vias oriented substantially normal to the first conducting plane and first conducting pad and disposed therebetween, each via of the cluster having a first end and a second end, wherein the first and second ends are physically connected respectively to the first conducting plane and first conducting pad; and

a second conducting pad disposed in a fourth substantially parallel plane internal to the region between the first and second conducting planes;

a second cluster of vias oriented substantially normal to the second conducting plane and second conducting pad and disposed therebetween, each via of the cluster having a first end and a second end, wherein the first

and second ends are physically connected respectively to the second conducting plane and second conducting pad andwherein the first and second conducting pads are proximate and capacitively coupled to each other; and

wherein a preselected reactance of the cluster resonator forms, over a desired frequency range, an electromagnetic shunt circuit between the first and second conducting planes.

69. (Previously presented) The cluster resonator of claim 68, wherein the vias of the clusters of vias are disposed along a common perimeter thereby forming substantially field free interior regions therewithin; and

wherein one or more electrically isolated interior vias traverse the interior regions of the clusters of vias, the interior vias comprising portions of transmission lines for passing electrical signals therethrough.

70 (Previously presented) The cluster resonator of claim 69 wherein a spacing of the vias of the clusters of vias in relation to the interior vias is selected to effect a predetermined line impedance in the interior vias.

71. (Previously presented) The cluster resonator of claim 69, wherein a diameter of the vias of the clusters of vias is selected to effect a predetermined inductance.

72. (Previously presented) The cluster resonator of claim 69, wherein the common perimeter is circular.

73. (Previously presented) The cluster resonator of claim 69, wherein the common perimeter is elliptical.

74. (Previously presented) The cluster resonator of claim 69 wherein the common perimeter is polygonal.

75. (Previously presented) The cluster resonator of claim 69, wherein the first and second conducting planes are metallic layers incorporated within a multi-layered panel circuit.

76. (Previously presented) The cluster resonator of claim 75, wherein the multi-layered panel circuit is a multi-layered printed circuit board and the cluster resonator comprises an array of plated through holes.

77. (Previously presented) The cluster resonator of claim 75, wherein the multi-layered panel circuit is a multi-chip module.

78. (Previously presented) The cluster resonator of claim 75, wherein the multi-layered panel circuit is a semiconductor chip.